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If no title is shown please refer to the description.
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Dielectric materials

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DIELECTRIC MATERIALS

The present invention generally relates to dielectric
materials and particularly relates to dielectric materials for
5 semiconductor switch devices.

Conventional semiconductor switch devices for very large scale
integration (VLSI) applications include complementary metal
oxide semiconductor (CMOS) switches. A CMOS switch typically
10 comprises a field effect transistor having a conduction
channel extending in a silicon substrate between a source
electrode and a drain electrode. A gate electrode is disposed
on the substrate between the source and drain. Conventionally,
the gate electrode is insulated from the channel by a gate
15 dielectric layer of silicon dioxide. In operation, the flow of
current through the channel between the source and drain is
controlled by application of voltage to the gate.

To date, the performance of microprocessors based on CMOS
20 technology has increased with time in a substantially
exponential fashion. This continuing increase in
microprocessor performance has been at least partially
facilitated by continuing reductions in CMOS device feature
size. The thickness of the gate dielectric is reduced in
25 correspondence to reduction in feature size. However, as the
feature size is reduced beyond 0.1 micro-metre, the thickness
of the gate dielectric becomes so small that electrical
breakdown occurs between the gate and channel where silicon
dioxide is employed the gate dielectric material. Upon
30 breakdown, the gate dielectric layer becomes electrically
conductive. Clearly, this effect is undesirable, and places a
lower limit on the degree to which CMOS devices can scaled
with silicon dioxide as the gate dielectric material.
Accordingly, it would be desirable to provide a dielectric
35 alternative to silicon dioxide that permits continuing
reduction in device feature size and thus a continuing
increase in microprocessor performance. Silicon dioxide has a
static dielectric constant (K) of around 4.0. It would be

desirable to provide a gate dielectric material having a K
value substantially higher than that of silicon dioxide. Such
a material would permit thinner gate dielectric layers than
presently possible with silicon dioxide while preserving
5 current CMOS semiconductor technology. Gate dielectric layers
of a thickness in the region of 2 nm or less would be
preferable.

Al_2O_3 is one material that has been investigated as an
10 alternative gate dielectric material for replacing silicon
dioxide. The K value associated with Al_2O_3 is about 10.
However, a problem associated with Al_2O_3 is that it introduces
a significant decrease in charge carrier mobility with respect
to silicon dioxide. Another problem associated with Al_2O_3 as a
15 gate dielectric material is that it is susceptible to boron
diffusion. Boron is regularly employed as a dopant in CMOS
devices for producing Ohmic contacts and the like. Diffusion
of boron into the gate dielectric layer produces an unwanted
degradation of the dielectric properties of the gate
20 dielectric layer. In addition, a layer of silicon dioxide
typically forms at the interface between the Al_2O_3 and the
silicon. This silicon dioxide layer further reduces the
effective K value. These problems have generally discouraged
further efforts into investigating Al_2O_3 as a replacement for
25 silicon dioxide as a gate dielectric materials for CMOS
devices.

In accordance with the present invention, there is now
provided an article of manufacture comprising a substrate and
30 a layer of $N_{(x)}Y_{(1-x)}AlO_3$ on the substrate where x is a molar
fraction greater than zero and less than one, and N is an
element selected from La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy,
Ho, Er, Tm, Yb, and Lu. In preferred embodiments of the
present invention, N is La. The layer preferably has a
35 rhombohedral perovskite structure. In particularly preferred
embodiments of the present invention, the layer has an average
dielectric constant value between 15 and 35. The molar
fraction x is preferably greater than 0.07. However, in

particularly preferred embodiments of the present invention, x
is less than 0.4. In some applications of the present
invention, an electrode may be electrically isolated from the
substrate by the layer. Examples of such applications include
5 electronic devices such as field effect transistors in which
the layer is especially suited to isolating the gate electrode
from conduction channel. The layer may be formed on the
substrate via molecular beam epitaxy.

10 In a preferred embodiment of the present invention, there is
provided a gate dielectric material comprising an alloy of
LaAl and YAl Oxides. Rhombohedral forms of this alloy
advantageously have an average K value of around 25 to 30.
Also, such forms of this alloy have a relatively high spatial
15 anisotropy. The relatively high spatial anisotropy leads to a
very high K value of around 50 in a direction extending
perpendicular to the channel. This direction will hereinafter
be referred to as the "Z direction". In addition, the alloy
provides sufficiently hard phonons in a plane perpendicular to
20 the Z direction. Such phonons prevent mobility decreases due
to phonon scattering. Furthermore, the alloy exhibits improved
thermodynamic stability and good interfacial properties with
silicon.

25 Preferred embodiments of the present invention will now be
described, by way of example only, with reference to the
accompanying drawings, in which:

Figure 1 is a graph of theoretical average K value against
30 percentage molar fraction of lanthanum for orthorhombic and
rhombohedral perovskite structures of $La_{(x)}Y_{(1-x)}AlO_3$;

Figure 2 is a graph of actual K value in the Z direction
against percentage molar fraction of lanthanum for perovskite
35 structures of $La_{(x)}Y_{(1-x)}AlO_3$;

Figure 3 is a graph of differential cohesion energy against percentage molar fraction of lanthanum for perovskite structures of $La_{(x)}Y_{(1-x)}AlO_3$;

5   Figure 4 is a graph of theoretical K value in the z direction against percentage molar fraction of lanthanum for orthorhombic and rhombohedral perovskite structures of $La_{(x)}Y_{(1-x)}AlO_3$;

10 Figure 5 is an isometric view of the atomic structure of rhombohedral $La_{0.1}Y_{0.9}AlO_3$.

Figure 6 is cross sectional view of a CMOS field effect transistor.

15

Experiments indicate that a stoichiometric alloy of Al_2O_3 and Y_2O_3 produces a crystalline solid solution $YAlO_3$ (YAP) with an orthorhombic perovskite structure and a K value of around 15. $YAlO_3$ is probably isotropic. In addition, Y_2O_3/Si(1 0 0)

20 interfaces have good electrical properties. By contrast, a stoichiometric alloy of Al_2O_3 and La_2O_3 produces a crystalline solid solution $LaAlO_3$ (LAR) with a rhombohedral perovskite structure and a K value of around 26. $LaAlO_3$ is probably highly anisotropic. However, La_2O_3/Si(1 0 0) interfaces do not have

25 good electrical properties. Despite this, we have found that alloys of $YAlO_3$ and $LaAlO_3$ have surprisingly desirable dielectric qualities. These qualities will now be described in detail.

30 Referring to Figure 1, curve 1 demonstrates the theoretical average K value of $La_{(x)}Y_{(1-x)}AlO_3$ in orthorhombic perovskite structure as a function of La concentration. Curve 2 demonstrates the theoretical K value of $La_{(x)}Y_{(1-x)}AlO_3$ in rhombohedral perovskite structure as a function of La

35 concentration. Curves 1 and 2 demonstrate that the K value of the rhombohedral structure is much greater than that of the orthorhombic structure throughout the composition range.

Turning to Figure 2, curve 3 demonstrates variation the actual
K value in the Z direction of $La_{(x)}Y_{(1-x)}AlO_3$ perovskite
structures as a function of La concentration. Below a
relatively low concentration of La, around 7%, the
5 rhombohedral structure of $La_{(x)}Y_{(1-x)}AlO_3$ is unstable.
Accordingly, below around 7% La concentration, $La_{(x)}Y_{(1-x)}AlO_3$
assumes the orthorhombic structure. As demonstrated by curve
3, $La_{(x)}Y_{(1-x)}AlO_3$ in orthorhombic form exhibits a relatively low
K value in the Z direction. However, at around 7% La
10 concentration, the rhombohedral form of $La_{(x)}Y_{(1-x)}AlO_3$
stabilizes. As demonstrated by curve 3, $La_{(x)}Y_{(1-x)}AlO_3$ in
rhombohedral form exhibits a significantly higher K value in
the Z direction. Accordingly, there is a significant step in
curve 3 corresponding to the transition between the
15 orthorhombic and rhombohedral phases of $La_{(x)}Y_{(1-x)}AlO_3$ at around
7% La concentration. Curve 3 demonstrates that Yttrium rich
rhombohedral perovskites exhibit highly anisotropic dielectric
properties in the Z direction.

20 A further understanding of the aforementioned transition
between rhombohedral and orthorhombic phases can be obtained
from Figure 3, in which curve 4 demonstrate the difference in
cohesive energy ΔE_{coh} between the rhombohedral and orthorhombic
phases of $La_{(x)}Y_{(1-x)}AlO_3$ as a function of La concentration. At
25 relatively low La concentrations, less than around 7% La, ΔE_{coh}
is positive, corresponding to stability in the orthorhombic
structure. However, higher La concentrations, beyond around 7%
La, ΔE_{coh} is negative, corresponding to stability in the
rhombohedral structure. The zero crossing point of curve 4
30 corresponds to a K value of around 50 in the Z direction. A
further demonstration of the surprisingly high dielectric
properties of Y rich rhombohedral $La_{(x)}Y_{(1-x)}AlO_3$ in the Z
direction is provided in Figure 4 in which curve 5 corresponds
to rhombohedral $La_{(x)}Y_{(1-x)}AlO_3$ and curve 6 corresponds to
35 orthorhombic $La_{(x)}Y_{(1-x)}AlO_3$.

Quaternary $La_{(x)}Y_{(1-x)}AlO_3$ alloys with Y concentrations in the
range 70 to 90 % and La concentrations correspondingly in the

range 30 to 10 % have particularly preferred characteristics
relative to other dielectric oxides investigated to date.
Polycrystalline formations of $La_{(x)}Y_{(1-x)}AlO_3$ exhibit surprisingly
high dielectric constants, thermodynamic stability, and good
5 electric properties at the interface with silicon. In the
interests of optimizing dielectric performance, $La_{(x)}Y_{(1-x)}AlO_3$ is
preferably grown epitaxially. Molecular Beam Epitaxy is one
particularly preferred growth technique. However, it will be
appreciated that other growth techniques may be employed.
10 Epitaxial growth is preferred because the polycrystalline
structure thus produced limits soft-phonons to the direction
of epitaxial growth. Without such limitation, dielectric
screening and phonon scattering of in plane electrons degrade
performance. However, it will be appreciated that the present
15 invention extends to amorphous formations of $La_{(x)}Y_{(1-x)}AlO_3$.

Referring to Figure 5, depicted therein is the atomic
structure of $La_{0.1}Y_{0.9}AlO_3$. Atomic sites 7 denote positions
occupied by oxygen atoms. Atomic sites 8 denote positions
20 occupied by aluminum atoms. Atomic sites 9 denote positions
occupied by either Yttrium atoms with a probability of 90% or
lanthanum atoms with probability of 10%.

With reference now to Figure 6, an example of a CMOS field
25 effect transistor (FET) embodying the present invention
comprises a silicon substrate 10. A conduction channel 11
extends through substrate 10 between a source (S) electrode 12
and a drain (D) electrode 13. A gate (G) electrode 14 is
disposed on the substrate 10 between the source electrode 12
30 and the drain electrode 13. In particularly preferred
embodiments of the present invention, the source electrode 12
and the drain electrode 13 comprise ohmic contacts. The gate
electrode 14 is electrically insulated from the channel 11 by
a gate dielectric layer 15. The gate dielectric layer 15 is
35 formed from a rhombohedral perovskite structure of
$La_{(x)}Y_{(1-x)}AlO_3$, where x is a molar fraction, preferably with a La
concentration close to 10%. In operation, the flow of current
through the channel 11 between the source electrode 12 and the

drain electrode 13 is controlled by application of voltage to
the gate electrode 14. It will be appreciated that the present
invention is applicable to both n channel and p channel FET
devices.

5

Preferred embodiments of the present invention have been
hereinbefore described with reference to $La_{(x)}Y_{(1-x)}AlO_3$ as a
dielectric material. However, the present invention is not
limited to the inclusion of La in $La_{(x)}Y_{(1-x)}AlO_3$. The present
10 invention equally contemplates replacing La in $La_{(x)}Y_{(1-x)}AlO_3$
with another element of the lanthanide series. Accordingly, in
other embodiments of the present invention, any of Ce, Pr, Nd,
Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu may be
substituted for La in $La_{(x)}Y_{(1-x)}AlO_3$.

15

In addition, although preferred embodiments of the present
invention have been hereinbefore described with respect to a
field effect transistor device, it will be appreciated that
the present invention is equally applicable to other articles
20 of manufacture in which a dielectric material is disposed on a
substrate. Such articles include for example electrical charge
storing devices such a capacitors. Many other applications are
possible.

25 In summary, described herein by way of example of the present
invention is an article of manufacture comprising a substrate
and a layer of $N_{(x)}Y_{(1-x)}AlO_3$ on the substrate where x is a molar
fraction greater than zero and less than one, and N is an
element selected from La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy,
30 Ho, Er, Tm, Yb, and Lu. The article may be an electronic
device further comprising an electrode electrically isolated
from the substrate by the layer. In particular, the dielectric
properties of the layer are such that the layer is especially
although be no means exclusively useful for electrically
35 isolating gate electrodes in field effect transistor devices.
The layer may be formed on the substrate via molecular beam
epitaxy.

CLAIMS

1.   Article of manufacture comprising a substrate and a layer of $N_{(x)}Y_{(1-x)}AlO_3$ on the substrate where x is a molar fraction greater than zero and less than one, and N is an element selected from La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu.

2.   Article as claimed in claim 1, wherein N is La.

3.   Article as claimed in claim 1 or claim 2, wherein the layer has a rhombohedral perovskite structure.

4.   Article as claimed in claim 3, wherein the layer has an average dielectric constant value between 15 and 35.

5.   Article as claimed in any of claims 2 to 4, wherein x is greater than 0.07.

6.   Article as claimed in claim 5, wherein x is less than 0.4.

7.   Article as claimed in any preceding claim, further comprising an electrode electrically isolated from the substrate by the layer.

8.   Electronic device comprising an article as claimed in claim 7.

9.   Field effect transistor device comprising an article as claimed in claim 7, wherein the electrode is the gate of the field effect transistor device.

10.   Method of manufacturing an article of manufacture as claimed in any of claims 1 to 7 comprising forming the layer on the substrate via molecular beam epitaxy.
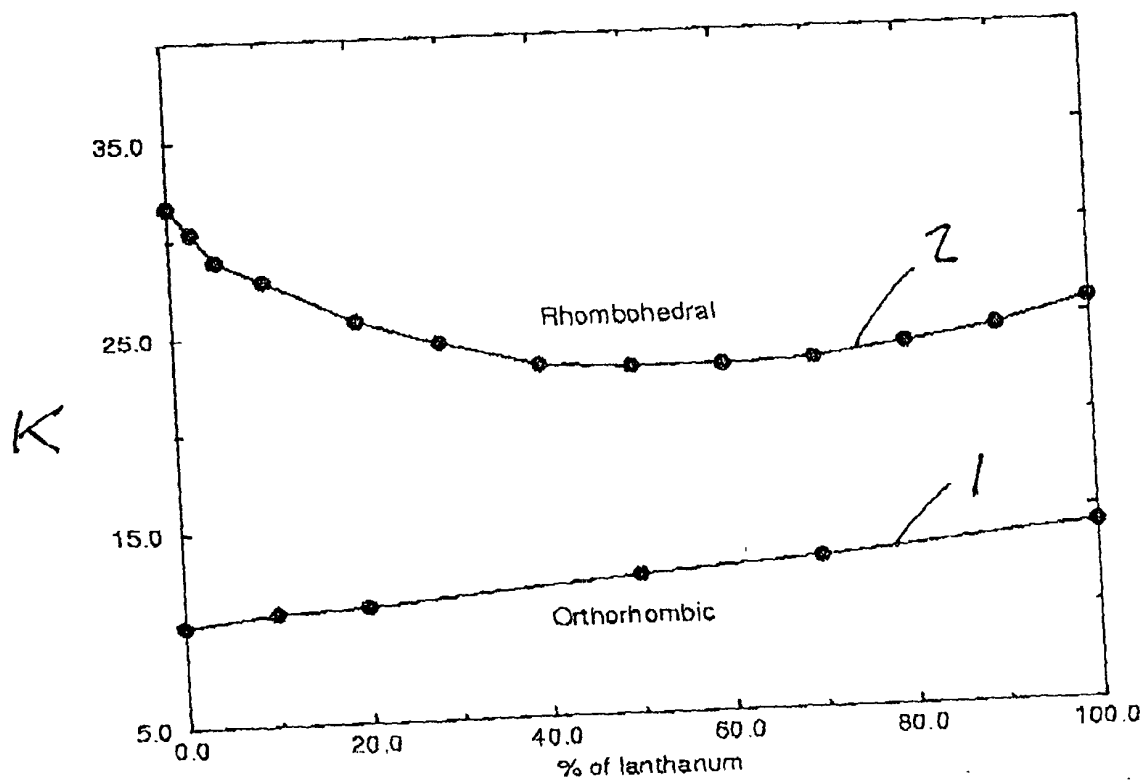
ABSTRACT

An article of manufacture comprises a substrate and a layer of
$N_{(x)}Y_{(1-x)}AlO_3$ on the substrate where x is a molar fraction
5 greater than zero and less than one, and N is an element
selected from La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er,
Tm, Yb, and Lu. The article may be an electronic device
further comprising an electrode electrically isolated from the
substrate by the layer. In particular, the dielectric
10 properties of the layer are such that the layer is especially
although by no means exclusively useful for electrically
isolating gate electrodes in field effect transistor devices.
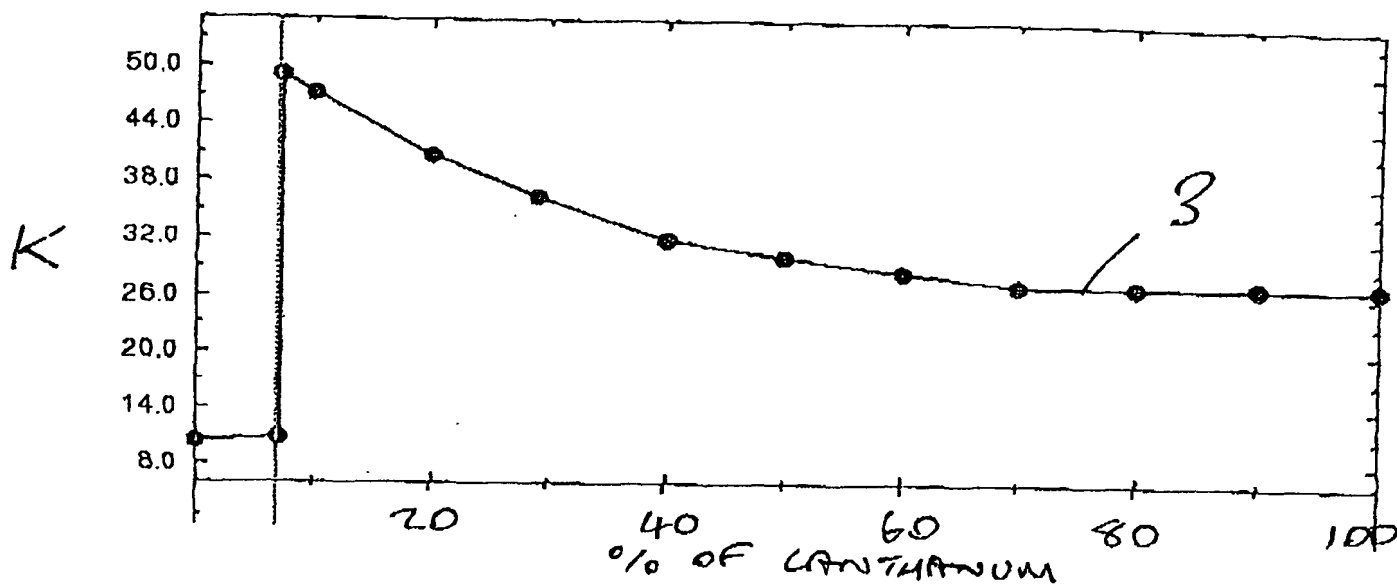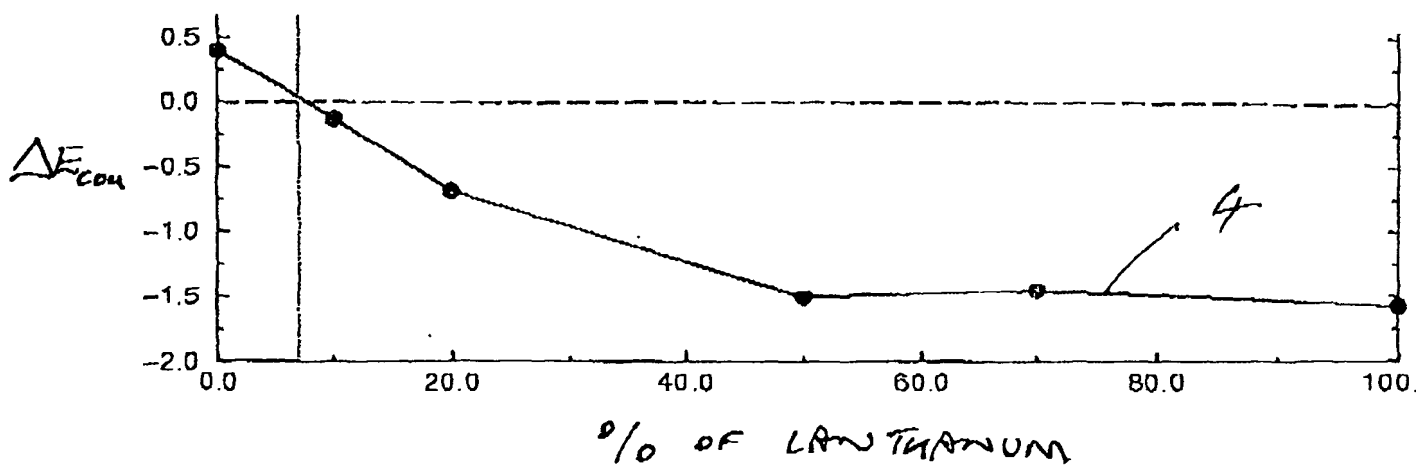The layer may be formed on the substrate via molecular beam
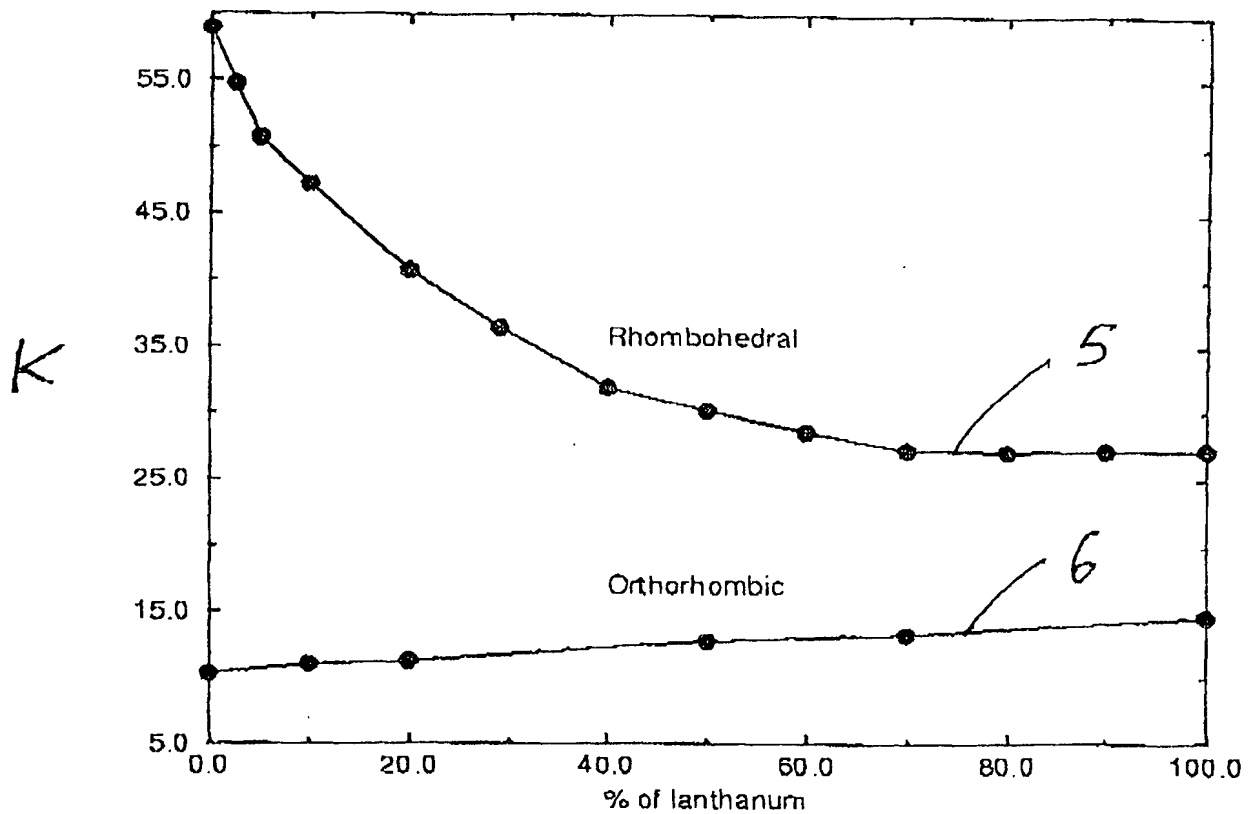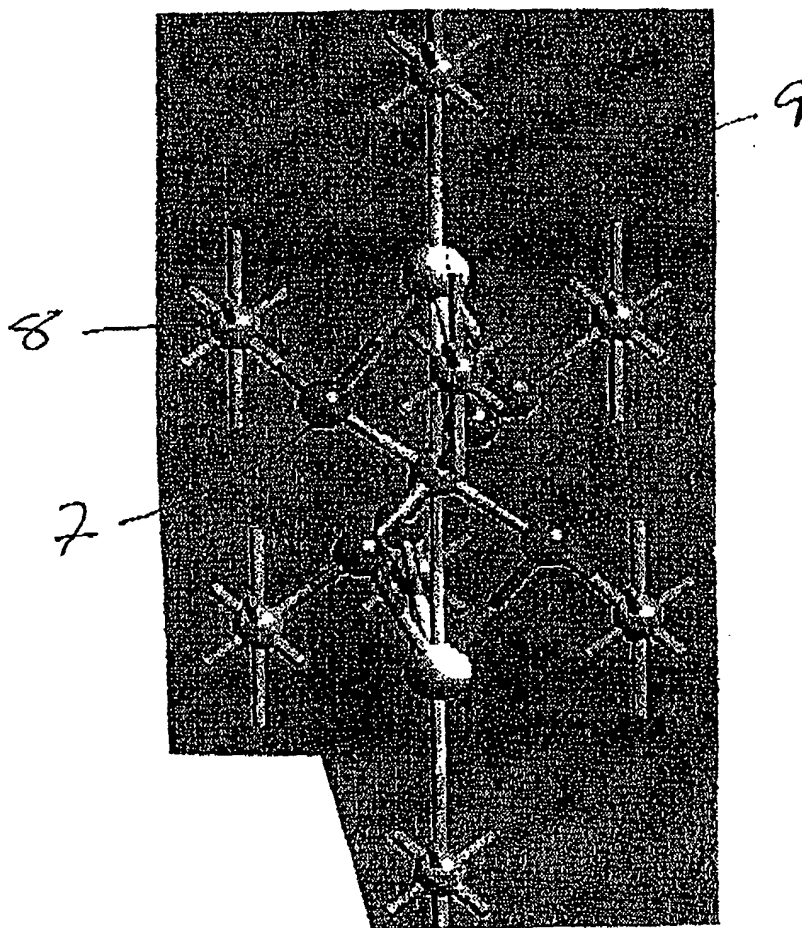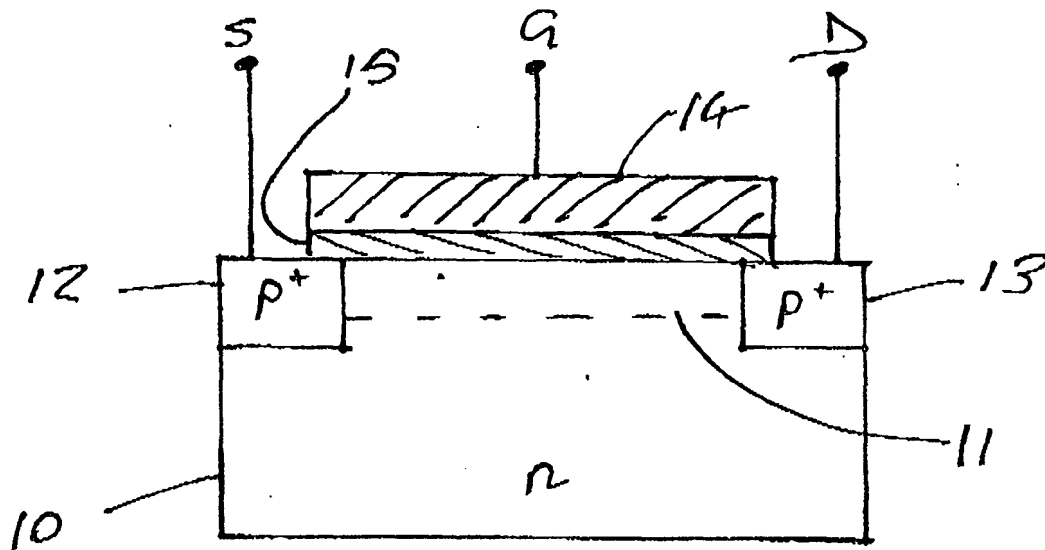epitaxy.

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FIG. 1

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FIG. 2

FIG. 3

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FIG. 4

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FIG.5

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S   G   D

15   14

12   P+   P+   13

10   n   11

FIG. 6